REMARKS

Claims 1-17 and 19-24 are pending in the present application. Claims 1-17 and 19-24 stand rejected.

Claim Objections

Claims 4-5, 13-15, 20-21 and 23 stand objected to because of informalities. Applicant has determined that the objection to Claim 5 should be an objection to Claim 6. Claims 4, 6, 13-15, 20-21 and 23 have been amended to correct these informalities and do not change the scope of the claims.

35 U.S.C. § 102 Rejections

Claims 1-6, 9-14 and 18-19 stand rejected under 35 U.S.C. 102(e) as being anticipated by Schnell (U.S. Pat. No. 6,137,327).

Claim 1 recites a method including receiving a first clock signal; providing a distributed clock signal to a clock distribution network having a plurality of endpoints connected to a respective plurality of components; and modifying the distributed clock signal until a portion of the distributed clock signal received at a first end point of the plurality of endpoints is substantially synchronized to the first clock signal (emphasis added). The Office indicates at section 7 of the Office Action that the portions of claim 1 with emphasis are disclosed in FIG. 5 of Schnell. Specifically, the Office indicates that a portion of the distributed clock received at a first endpoint, represented by one of the DQ-Pads of Schell, is substantially synchronized to a first clock signal, represented by FB_CLK. The Applicant respectfully disagrees.

As identified by the Office, Schnell does not disclose a distributed clock signal received at a first end point of the plurality of endpoints that is substantially synchronized to the first clock signal. Instead, the distributed clock signal received at the first endpoint (one of the DQ-Pads) is purposefully skewed (i.e., not substantially synchronous) from the first clock (FB_CLK)

by a delay introduced through Schnell's interface logic SSTL_IF 106, receiver RCV 102, and Package RC_Delay_M. Note that the distributed clock signal of Schnell (OCD-DLLCLK) received the first endpoint of Schnell (DQ-Pads) is skewed relative to FB_CLK effectively by the same amount as the distributed clock signal received at the endpoint that is connected to the input side of logic block 106 (SSTL_IF).

Because Schnell neither discloses nor suggests a method as recited in Claim 1, Claim 1 is necessarily not anticipated and non-obvious over Schnell. For this reason, withdrawal of the rejection of Claim 1 is requested, and allowance of independent Claim 1 is respectfully solicited. Claims 2-12 depend from allowable Claim 1 and are allowable for at least this reason. In addition, claims 2-12 include additional non-obvious, patentable subject matter.

Amended Claim 13 recites a method including providing a first clock signal from a first device; receiving a representation of the first clock signal from a device external to the first device at the first device; providing the representation of the first clock signal to a delay element; providing a delayed clock signal from the delay element to a clock distribution tree, wherein the delayed clock signal is based upon the representation of the first clock signal, and the clock distribution tree includes a plurality of leaves that provide the delayed clock signal to a respective plurality of components; providing a representation of the delayed clock signal from a first leaf to the delay element, where the first leaf is one of the plurality of leaves; and modifying the delayed clock signal provided by the delay element based upon the representation of the delayed clock signal from the first leaf.

Clarification by the Office of the rejection of Claim 13, or its allowance is respectfully requested. Specifically, the Office identifies at section 14 of the Office Action the recited first clock signal as clock output 112 (from device 110), and the recited representation of the first clock signal from external the first device as REFCLK (from receiver 116). However, REFCLK is not a representation of the clock output 112 (first clock). For this reason, withdrawal of the rejection of claim 13 under § 102, and its allowance is requested. In addition, Claim 14 depends from allowable Claim 13 and is allowable for at least this reason. Claim 14 includes additional non-obvious patentable subject matter.

Claims 15-17 stand rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (U.S. Pat. No. 6,446,180) (hereinafter "Li").

Amended Claim 15 recites a method including generating a first clock edge at a first device at a first time, wherein the first clock edge is associated with a first clock having a first period; receiving the first clock edge at a second device at a second time, wherein the time between the first time and the second time is a first propagation delay; generating a data signal at the second device at a third time in response to receiving the first clock edge, wherein the time between the second time and the third time is a second propagation delay; receiving the data signal at a first component of the first device at a fourth time, wherein the time between the third time and the fourth time is a third propagation delay; providing a representation of the first clock to a delay component of the first device, wherein the representation of the first clock is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first, second and third propagation delays; generating a distributed clock from the delay component to drive a clock distribution network having a plurality of endpoints; receiving at the delay component a representation of the distributed clock at a first endpoint of the plurality of endpoints; and modifying the distributed clock until the representation of the distributed clock at the first endpoint is synchronized with the representation of the first clock (emphasis added).

Li does not disclose generating a clock and receiving the data signal at a first device as recited. Because Li neither discloses nor suggests a method as recited in Claim 15, Claim 15 is necessarily not anticipated and non-obvious over Li. For this reason, withdrawal of the rejection of Claim 15 is requested, and allowance of independent Claim 15 is respectfully solicited. Claims 16-17 depend from allowable Claim 15 and are allowable for at least this reason. Claims 16-17 include additional non-obvious patentable subject matter.

35 U.S.C. § 103 Rejections

Claims 6-8, 11-12, 15-17 and 20-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell. No specific rejection of claim 15 is made in the Office Action with regards to § 103, but instead, the rejection of claim 15 appears to have been a § 102 rejection.

Claim 20 has been rewritten as an independent claim. The scope of Claim 20 has not been changed. Claim 18 has been canceled without prejudice or disclaimer. Claim 20 has been rejected under § 103 based on Schnell.

Claim 20 recites an apparatus including a delay locked loop having a reference input, a feedback input, and a delayed reference output; and a distribution network having a first node connected to the delayed reference output, a plurality of end nodes connected to a respective plurality of components, a first end node of the plurality of end nodes connected to the feedback input of the delay locked loop, where the delay locked loop is one of the plurality of components, a first input port having an output node coupled to the reference input of the delay locked loop, and an input node, wherein the first input port, the distribution network, and the delay locked loop are formed on a first substrate; a first trace connected to the input node of the first input port, wherein the first trace is formed on the second on a second substrate which is different than the first substrate; and a first output port having an output node coupled to the first trace, wherein the output port is formed on the first substrate.

Claim 20 recites, in part, a first input port having an output node and an input node. The Office states that receiver 116 is an input port. The Applicant respectfully disagrees. There is no indication in Schnell that the receiver 116 is an input port as recited, nor does Schnell suggest that the receiver 116 is connected to a first trace format on a second substrate while the first input port is formed on a first substrate. The fact that there is no first trace on a second substrate supports the fact that the receiver 116 is not an input port as recited. The Office acknowledges that Schnell does not disclose a first and second substrate as recited, and states that it would have been obvious to modify Schnell by using the apparatus of Schnell in an environment where the first trace of Schnell is routed on a second substrate different than the first substrate to compensate for technology and temperature effects taught by Schnell. However, Schnell does not disclose nor suggest coupling the reference input of a delay locked loop to an external trace as recited. The generic mention of avoiding deviations in delay due to technology and temperature as recited by the Office, does not lead one of ordinary skill to the specific recitations of multiple substrates of claim 20. The advantage of such a routing is that it allows for a matching of the cumulative trace length of the paths 34 and 32 to compensate for static variations

in the printed circuit board that otherwise cannot otherwise be compensated for (see first full paragraph of page 7 of application). Schnell provides no such motivation.

Claims 23-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Li.

Amended Claim 23 recites a method including providing a first clock signal from a first device, wherein the first clock signal is transmitted over a first substrate to a second device, wherein the first substrate is not part of the first device or the second device; providing a second clock signal from the first device, wherein the second clock signal is transmitted over a second substrate, wherein the second substrate is not part of the first device or the second device; receiving the second clock signal at a delay component of the first device as a modified second clock signal; receiving a third signal at a storage component, in response to the first clock signal, wherein a latching signal is based upon the modified second clock signal and a previous latching signal from the delay component; and latching the third signal at the storage component based upon the latching signal.

Li does not disclose the first substrate, the second substrate, the first device or the second device as recited. The Office states that Li does not expressly limit his invention to working with any devices on a particular substrate. Applicant respectfully disagrees. The components of FIG. 2 of Li, used to reject claim 23, are all part of a single memory device 30, and therefore reside on a common substrate. Even if no contrary showing existed within Li, the burden of showing a motivation to combine references, or to add features not in a reference, is a burden to be met by the Office based on the references. The fact that a reference is silent does not meet this burden. For this reason, it is respectfully requested that the rejection of claim 23 be withdrawn.

For at least the reasons stated above, Claim 23 is necessarily not anticipated and non-obvious over Li. For this reason, withdrawal of the rejection of Claim 23 is requested, and allowance of independent Claim 23 is respectfully solicited. Claim 24 depends from allowable Claim 23 and is allowable for at least this reason. Claim 24 includes additional patentable subject matter.

Applicant respectfully submits that the present application is now in condition for allowance. Accordingly, the Examiner is requested to issue a Notice of Allowance for all pending claims.

Should the Examiner deem that any further action by the Applicant would be desirable for placing this application in even better condition for issue, the Office is requested to issue a formal Notice of Allowance for all pending claims.

Respectfully submitted,

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